Claims

[c1] A flip-flop comprising:

a first latch for receiving at least one bit;

a second latch coupled to the first latch for storing the at least one bit from the first latch, wherein the size of the second latch is minimized to reduce power consumption; and

a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a clock to the multiplexor is active and for outputting the at least one bit from the second latch when the clock is inactive.

[c2] The flip-flop of claim 1 wherein the multiplexor is a shunt multiplexor.

[c3] The flip-flop of claim 1 wherein a first clock causes the at least one bit to be provided from the first latch to the multiplexor and the second latch.

[c4] The flip-flop of claim 1 wherein the first latch is a master latch.

[c5] The flip-flop of claim 3 wherein the second latch is a slave latch.

[c6] A flip-flop comprising:

a master latch for receiving at least one bit; and

a slave latch coupled to the master latch for storing the at least one bit from the master latch wherein the size of the slave latch is minimized to reduce power consumption; and

a multiplexor coupled to the master latch and to the slave latch for outputting the at least one bit from the master latch when a clock to the multiplexor is active and for outputting the at least one bit from the slave latch when the clock is inactive.

[c7] The flip-flop of claim 1 wherein a first clock causes the at least one bit to be provided from the master latch to the multiplexor and the slave latch.

[c8] A method for optimizing power and performance in a flip-flop, wherein the flip-flop includes a first latch and a second latch coupled to the first latch, the method comprising the steps of:

(a) receiving at least one bit into the first latch, wherein the first latch ouputs the at least one bit to the second latch and to a multiplexor when a first clock is active; and

(b) outputting the at least one bit received from the first latch from the multiplexor when a second clock is active; and

(c) outputting the at least one bit received from the second latch from the multiplexor when the second clock is inactive.

[c9] A flip-flop comprising:

a master latch for receiving at least one bit;

a slave latch coupled to the master latch for storing the at least one bit based upon a first clock from the master latch, wherein the size of the second latch is minimized to reduce power consumption; and

a shunt multiplexor coupled to the master latch and to the slave latch for receiving the at least one bit based upon the first clock, for outputting the at least one bit from the master latch when a second clock to the multiplexor is active, and for outputting the at least one bit from the slave latch when the second clock is inactive.